CLAIMS

1. An oscillator controller in an integrated circuit, comprising:

differential logic for receiving a differential clock input and a differential oscillator input, the differential clock input associated with a clock signal, the differential oscillator input associated with an oscillator signal, the clock signal and the oscillator signal having different frequencies;

the differential logic configured to provide a differential output at least partially responsive to at least one of the clock signal and the oscillator signal; and

control logic for receiving control signals, the control logic configured to put the differential logic in one of three states in response to the control signals, the three states including a first state for propagating by the differential logic an edge of the clock signal to the differential output for a hard-phase alignment.

2. The oscillator controller, according to claim 1, wherein the three states are for a pre-lock condition and a post-lock condition, the pre-lock condition being prior to frequency locking to the clock signal, and the post-lock condition being after frequency locking to the clock signal.

3. The oscillator controller, according to claim 2, wherein the first state occurs during the post-lock condition.

4. The oscillator controller, according to claim 3, wherein the three states include a second state for propagating by the differential logic the oscillator signal to the differential output.

5. The oscillator controller, according to claim 4, wherein the second state occurs during the post-lock condition.

6. The oscillator controller, according to claim 5, wherein the three states include a third state for propagating by the differential logic a control signal of the control signals to the differential output.

7. The oscillator controller, according to claim 6, wherein the third state occurs during the pre-lock condition.

8. The oscillator controller, according to claim 5, wherein the control signals comprise a first control signal and a second control signal; and wherein the first control signal transitions from a first voltage level to a second voltage level responsive to overlap between a concurrence signal and a reference concurrence signal to put the differential logic in the first state.

9. The oscillator controller, according to claim 8, wherein the second control signal transitions from the first voltage level to the second voltage level responsive to the differential logic transitioning from the pre-lock condition to the post-lock condition.

10. The oscillator controller, according to claim 9, wherein the first control signal and the second control signal are respectively provided to inverters in series to obtain phase control signals.

11. The oscillator controller, according to claim 9, wherein all of the control signals are obtained from the first control signal and the second control signal.

12. The oscillator controller, according to claim 9, wherein the differential logic is Differential Cascode Voltage Switch Logic formed entirely of n-type transistors.

13. An oscillator controller in an integrated circuit, comprising:

differential logic for receiving a differential clock input and a differential oscillator input, the differential clock input associated with a clock signal, the differential oscillator input associated with an oscillator signal, the clock signal and the oscillator signal having different frequencies;

the differential logic configured to provide a differential output at least partially responsive to at least one of the clock signal and the oscillator signal;

the differential logic configured to provide a combinational circuit in an oscillator alignment state and to provide a sequential circuit in a hard-phase alignment state; and

control logic for receiving control signals, the control logic in part to selectively alternate between putting the differential logic in the oscillator alignment state and in the hard-phase alignment state responsive to the control signals.

14. The oscillator controller, according to claim 13, wherein the differential logic is configured to propagate an edge of the clock signal to the differential output in the hard-phase alignment state and to provide feedback from the differential output representing a change in logic level responsive the edge propagated, the feedback provided asynchronously in advance of another edge of the clock signal immediately following the edge to prevent the other edge from being propagated to the differential output.

15. The oscillator controller, according to claim 14, wherein the control signals selectively cause the differential logic to transition from the hard-phase alignment state to the oscillator alignment state after the feedback is asynchronously provided to propagate the oscillator signal to the differential output.

16. The oscillator controller, according to claim 15, wherein the feedback establishes a signal state latch within the differential logic.

17. The oscillator controller, according to claim 16, wherein the differential logic is Differential Cascode Voltage Switch Logic formed entirely of n-type transistors.

18. The oscillator controller, according to claim 17, wherein the differential logic and the control logic are part of a digital clock management circuit.

19. The oscillator controller, according to claim 17, wherein the integrated circuit is a field programmable gate array.

20. An oscillator controller in an integrated circuit, comprising:

first means for receiving a differential clock input and a differential oscillator input, the differential clock input associated with a clock signal, the differential oscillator input associated with an oscillator signal, the clock signal and the oscillator signal having different frequencies;

the first means configured to provide a differential output at least partially responsive to at least one of the clock signal and the oscillator signal;

the first means configured to provide a combinational circuit in an oscillator alignment state and to provide a sequential circuit in a hard-phase alignment state;

second means for receiving control means, the second means in part for selectively alternating between putting the first means in the oscillator alignment state and in the hard-phase alignment state responsive to the control means.

21. An oscillator controller in an integrated circuit, comprising:

first means for receiving a differential clock input and a differential oscillator input, the differential clock input associated with a clock signal, the differential oscillator input associated with an oscillator signal, the clock signal and the oscillator signal having different frequencies;

the first means configured to provide a differential output at least partially responsive to at least one of the clock signal and the oscillator signal; and

second means for receiving control means, the second means configured to put the first means in one of three states in response to the control means, the three states including a first state for propagating by the first means an edge of the clock signal to the differential output for a hard-phase alignment.